REMARKS

The Office Action dated January 13, 2005, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 1, 6, 16 and 21 have been amended. Applicants submit that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1, 2 and 4-21 are pending in the present application and are respectfully submitted for consideration.

Claims 1-2, 4-5 and 16-21 Rejected Under 35 U.S.C. § 103(a)

Claims 1-2, 4-5 and 16-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Takahashi et al. (JP40927070) hereinafter "Takahashi"). Applicant traverses this rejection.

Claim 1 recites an input circuit comprising, among other features, a current regulating circuit connected to the second source of the second transistor and connected in parallel to the constant current source, wherein the current regulating circuit conditions an amount of the current flowing through the differential circuit to be increased in response to the node signal when the first transistor changes its state from an activated state to a deactivated state in response to the external signal and the node signal rises, such that only a rising delay time of the node signal is shortened.

Claim 16 recites an input circuit comprising, among other features, a first inverter having an input terminal connected to a second node between the first and fifth transistors and an output terminal connected to the gate of the fourth transistor, a node

signal having a rising edge and a falling edge is generated at the second node in accordance with a current flowing through the first and second transistors, and wherein the fourth transistor operates to condition an amount of the current flowing through the second transistor to be increased in response to the node signal when the first MOS transistor changes its state from an activated state to a deactivated state in response to the data signal and the node signal rises, such that only a rising delay time of the node signal is shortened.

Claim 21 recites a semiconductor integrated circuit comprising, among other features, a current adjustment transistor coupled to the sources of the first and second transistors, a third gate of the current adjustment transistor receiving the differential output signal of the differential circuit, wherein the current adjustment transistor operates to condition an amount of the current flowing through the differential circuit to be increased in response to the logic level of the differential output signal when the first transistor changes its state from an activated state to a deactivated state in response to the data strobe signal and the differential output signal rises, such that a rising delay time of the logic level of the differential output signal is shortened.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

Applicants submit that Takahashi fails to disclose or suggest each and every element recited in claims 1, 16 and 21 of the present application. In particular, Takahashi does not disclose at least a current regulating circuit that increases an amount of current flowing through a differential circuit when a node signal rises, as recited in claim 1; Takahashi does not disclose a fourth transistor that increases an

amount of current flowing through a differential circuit when a node signal rises, as recited in claim 16; and Takahashi does not disclose a current adjustment transistor that increases an amount of current flowing through a differential circuit when a differential output signal rises, as recited in claim 21.

Rather, as shown in Figs. 4 and 5 of the cited reference, Takahashi increases an amount of current flowing through a differential circuit by turning on the transistor N6 after the node signal n4 completely rises to a high level in order to lower the voltage of the node signal n4 from the high level by ΔV. In other words, Takahashi cannot increase an amount of current when the node signal n4 rises.

Therefore, Applicants submit that Takahashi fails to disclose each and every element recited in claims 1, 6 and 16 of the present application. In addition, it is submitted that the present invention is not obvious in view of Takahashi. Furthermore, one skilled in the art could not achieve the present invention from Takahashi for the purpose of shortening the rising time of a node signal.

To establish *prima facie* obviousness, each feature of a rejected claim must be taught or suggested by the applied art of record. See M.P.E.P. §2143.03 and *In re Royka*, 490 F.2d 981 (CCPA 1974). As explained above, Takahashi does not teach or suggest each feature recited by pending claims 1, 16 and 21. Accordingly, for the above provided reasons, Applicant respectfully submits that pending claim 1, 16 and 21 is not rendered obvious under 35 U.S.C. § 103 by the teachings of Takahashi. Therefore, it is respectfully submitted that claims 1, 16 and 21 are allowable.

Under U.S. patent practice, the PTO has the burden under §103 to establish a *prima facie* case of obviousness. In re Fine, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Both the case law of the Federal Circuit and the PTO itself have made clear that where a modification must be made to the prior art to reject or invalidate a claim under §103, there must be a showing of proper motivation to do so. The mere fact that a prior art reference could arguably be modified to meet the claim is insufficient to establish obviousness. The PTO can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. Id. In order to establish obviousness, there must be a suggestion or motivation in the reference to do so. See also In re Gordon, 221 USPQ 1125, 1127 (Fed. Cir. 1984) (prior art could not be turned upside down without motivation to do so); In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1998); In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Lee, 277 F.3d 1338 (Fed. Cir. 2002).

As claims 2, 4, 5 depend from claim 1, and claims 17-20 depend from claim 16, Applicant submits that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with respect to the independent claims, as well as for the additional subject matter recited therein.

Applicant respectfully requests withdrawal of the rejection.

Claim 6-20 Rejected Under 35 U.S.C. § 103(a)

Claims 6-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Figure 1 of Applicant's admitted prior art ("AAPA") in view of Takahashi. Applicant traverses this rejection.

Claim 6 recites a semiconductor integrated circuit comprising, among other features, a current regulating circuit, connected to the differential circuit, which

conditions an amount of the current flowing through the differential circuit to be increased in response to the node signal when the first transistor changes its state from an activated state to a deactivated state in response to the external signal and the node signal rises, such that only a rising delay time of the node signal is shortened.

In making the rejection, the Office Action admits that "Figure 1 of the admitted prior art ... does not discloses that the amplifiers have a current regulating circuit increases an amount of the current flowing through the differential circuit in response to the node signal such that only rising delay time of the node signal is shortened."

The Office Action relies on Takahashi to make up the deficient features.

As mentioned above, Takahashi does not disclose at least a current regulating circuit that increases an amount of current flowing through a differential circuit when a node signal rises, as recited in claim 1; and Takahashi does not disclose a fourth transistor that increases an amount of current flowing through a differential circuit when a node signal rises, as recited in claim 16.

To establish *prima facie* obviousness, each feature of a rejected claim must be taught or suggested by the applied art of record. See M.P.E.P. §2143.03 and *In re Royka*, 490 F.2d 981 (CCPA 1974). As explained above, Figure 1 of AAPA and Takahashi, taken alone or in combination, does not teach or suggest each feature recited by pending claims 6 and 16. Accordingly, for the above provided reasons, Applicant respectfully submits that pending claim 6 and 16 are not rendered obvious under 35 U.S.C. § 103 by the teachings of AAPA in view of Takahashi. Therefore, it is respectfully submitted that claims 6 and 16 are allowable.

As claims 7-15 depend from claim 6, and claims 17-20 depend from claim 16, Applicant submits that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with respect to the independent claims, as well as for the additional subject matter recited therein.

Applicant respectfully requests withdrawal of the rejection.

Conclusion

In view of the above, Applicants respectfully submit that each of claims 1, 2 and 4-21 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1, 2 and 4-21 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicant respectfully petitions for an appropriate extension of time.

Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300.

Respectfully submitted,

Sam Huang
Registration No. 48,430

Customer No. 004372
ARENT FOX, PLLC
1050 Connecticut Avenue, N.W., Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6000
Fax: (202) 857-6395

SH:vdb